<D5M Modify> Application Note

1.1 Introduction

设计是将 DE2_115_CAMERA 800x600 工程修改成分辨率为 1280x720 的工程，能够实现高分辨率采集图像，获得更大的图像，为开发者提供更灵活的相机参考配置。整体构架是基于 rtl 的硬件描述 ,将整个功能分成 5 个部分：1.VGA 控制部分。2.多口 SDRAM 控制部分。3.RAW TO RGB 部分。4.数据捕获部分。5.相机配置部分。

The design is used to modify the project with the resolution of 800x600 to 1280 x 720 in order to obtain high resolution image captured，large size image, to provide developer more flexible setting of the camera. The whole structure base on the RTL hardware description to devide the project to 5 parts: 1. VGA controller 2.multi-interface SDRAM controller 3.RAW to RGB section 4.CCD capture 5. D5M Configuration.

1.2 Function Description

■ Hardware

首先通过配置模块将摄像头配置成预设的采集规格，通过数据捕获器将传感器送回的图像资料有效收集，经过 raw to rgb 生成 RGB 像素点存放在 buffer 中，在从 buffer 中读取数据将其显示在显示器上，从而实现整个图像的采集和显示。详细组成如图 1 所示

First of all, the CCD camera is being set to be the caputer mode via configure modul，collect the data from the caputer, convert the raw to rgb and store the RGB pixels into buffer. Read the buffer and disply the image in the VGA display to complete the whole procedure of the image capture and display. The diagram1 below reflect the structure:

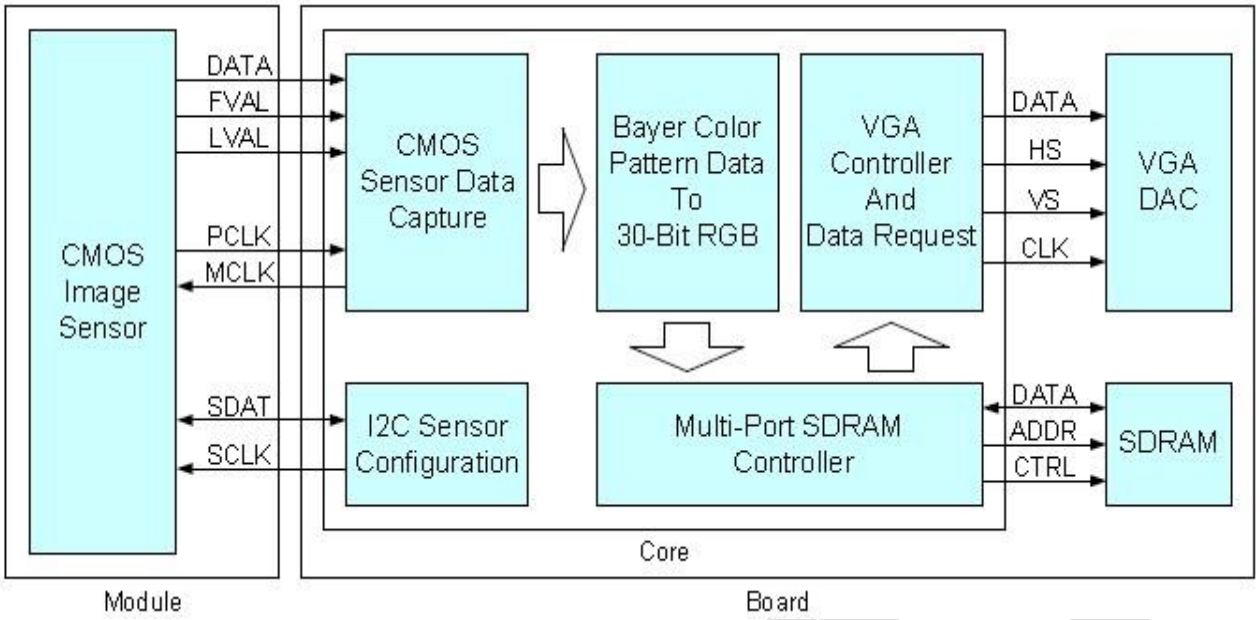


Diagram 1 Camera Structure

I²C 相机配置模块：模块通过 I²C 协议设置相应的功能寄存器，来预设图像采集的的规格，采集方式和对采集以后的数据的操作。

I²C Sensor Configuration: The modul is being used to set the corresponding function register through the I²C protocols to default the image specification, mothed and the operation on the data captured.

数据捕获器：传感器采集完数据以后会按照预设的方式发送数据，将采集的图像信号以行列的方式发送，在行有效期间会将行数据以 PCLK 的速度将行的每个数据发送出去，在捕获器这边需要在行场信号的控制下有效地将数据收集。

CMOS Sensor Data Capture: the sensor will send out the data by default after the data capture completed, the date is sent out in Line and Frame. If the LVAL is active, the data in line will be sent out with the speed of PCLK

多口 SDRAM 控制器：通过两个写 FIFO 和两个读 FIFO 与 SDRAM 控制组成，通过两个写 FIFO 将 RAW TO RGB 的的数据放入到 SDRAM 中，并且通过两个读 FIFO 将 SDRAM 中的数据读出送至 VGA 接口，其中 FIFO 的作用时钟匹配和控制 SDRAM 读写。

Muti-Port SDRAM Controller: Through two Write FIFO interface and two Read FIFO interface with the SDRAM controller making up, put the RAW TO RGB data into SDRAM from the Write FIFO interface, then send the data from SDRAM into VGA interface though Read FIFO interface,

The FIFO is used to Clock matching and the SDRAM Read & Write controller.

Raw to RGB 将：D5M 产生的序列数据通过 line buffer 来切割数据，然后将每一个像素点的 RGB 分离出来，重新生成 RGB 像素点的数据。

Raw to RGB module：The pixel array which D5M generated has been devided into 2 taps in the Line Buffer, then extract the R, G, B component from the pixel to rebuild the image.

VGA 控制器：生成标准 vga 接口的时序。

VGA Controller: The VGA controller is used to generate the timing of the VGA interface.

本例是用 DE2_115_CAMERA 800x600 工程修改具体修改参数如下所述：

Use the project of DE2_115_CAMERA 800x600 as an example, the user can refer to the instruction below for the concrete paremeters modification.

1. vga 参数修改

1. VGA parameter modification

在文件夹 V 中找到 VGA_Controller.v 档打开，参照标准的 VGA 参数表将 VGA 参数设置成为 1280X720，具体修改如下：

Open the VGA_Controller.v file, set the parameter as below for VGA resolution 1280x720 by referring to standard parameter table.

```
parameter H_SYNC_CYC = 51;

parameter H_SYNC_BACK = 25;

parameter H_SYNC_ACT = 1280;

parameter H_SYNC_FRONT= 20;

parameter H_SYNC_TOTAL= 1376;
```

```
// Virtical Parameter ( Line )

parameter V_SYNC_CYC = 2;

parameter V_SYNC_BACK = 11;

parameter V_SYNC_ACT = 720;

parameter V_SYNC_FRONT= 1;

parameter V_SYNC_TOTAL= 734;
```

同时将 VGA 的 clk 设为 60M。这样配置出来的 VGA 参数就是 1028X720p60 具体步骤如下：

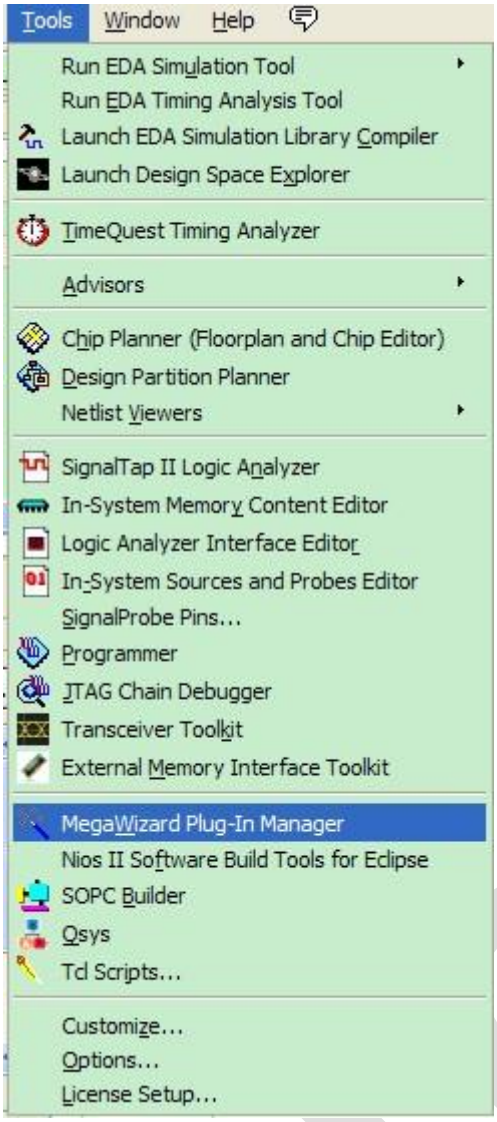
在 tools 栏找到 MegaWizard Plug-Manager 并打开。

Meanwhile, the VGA clock should be set to 60MHz.

Then the VGA parameters have be set as 1028X720p60 now.

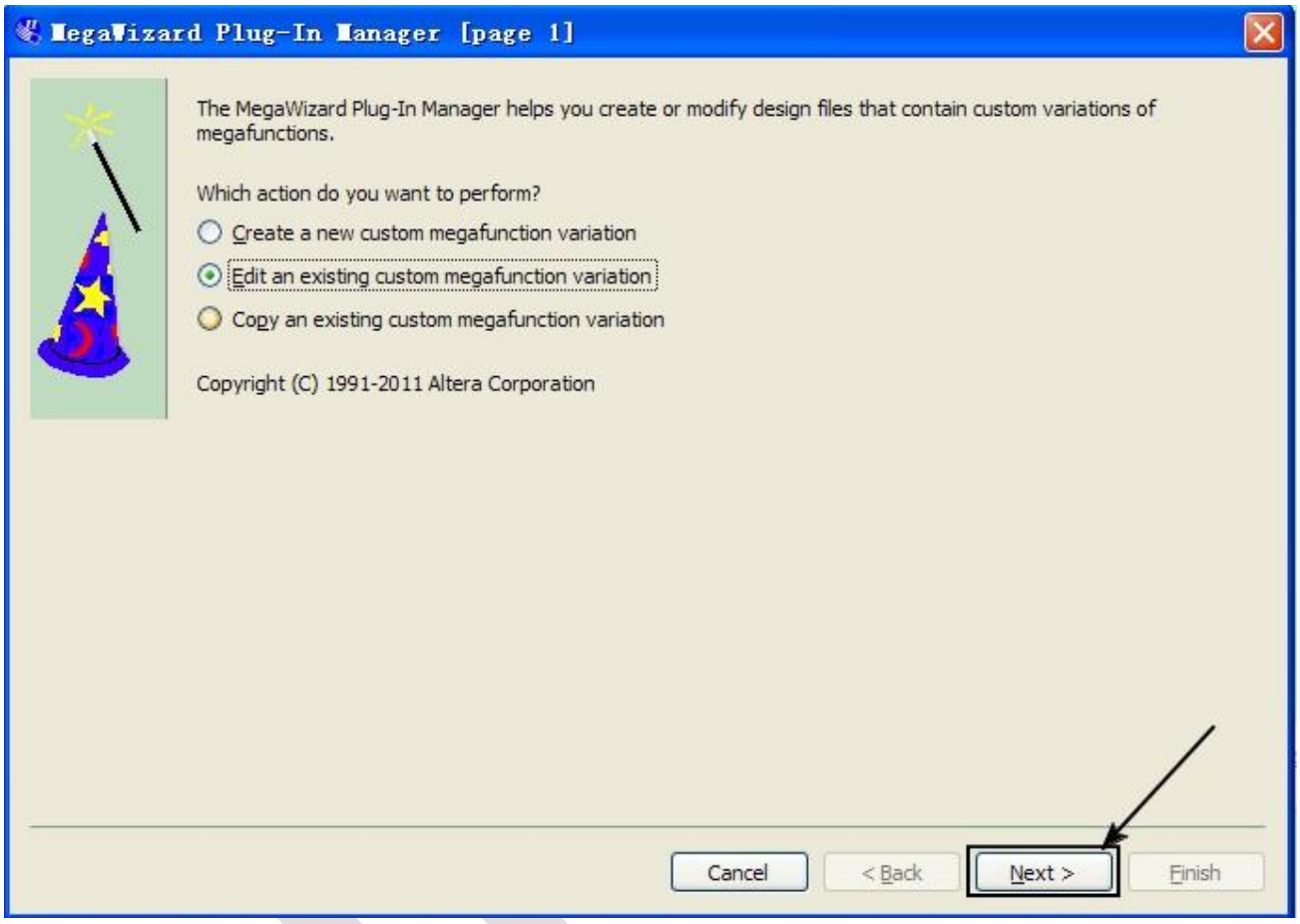
What is the procedure for achieving it?

Click Tool > MegaWizard Plug-Manager


Tools
Window
Help
Run EDA Simulation Tool
Run EDA Timing Analysis Tool
Launch EDA Simulation Library Compiler
Launch Design Space Explorer
TimeQuest Timing Analyzer
Advisors
Chip Planner (Floorplan and Chip Editor)
Design Partition Planner
Netlist Viewers
SignalTap II Logic Analyzer
In-System Memory Content Editor
Logic Analyzer Interface Editor
In-System Sources and Probes Editor
SignalProbe Pins...
Programmer
JTAG Chain Debugger
Transceiver Toolkit
External Memory Interface Toolkit
MegaWizard Plug-In Manager
Nios II Software Build Tools for Eclipse
SOPC Builder
Qsys
Tcl Scripts...
Customize...
Options...
License Setup...

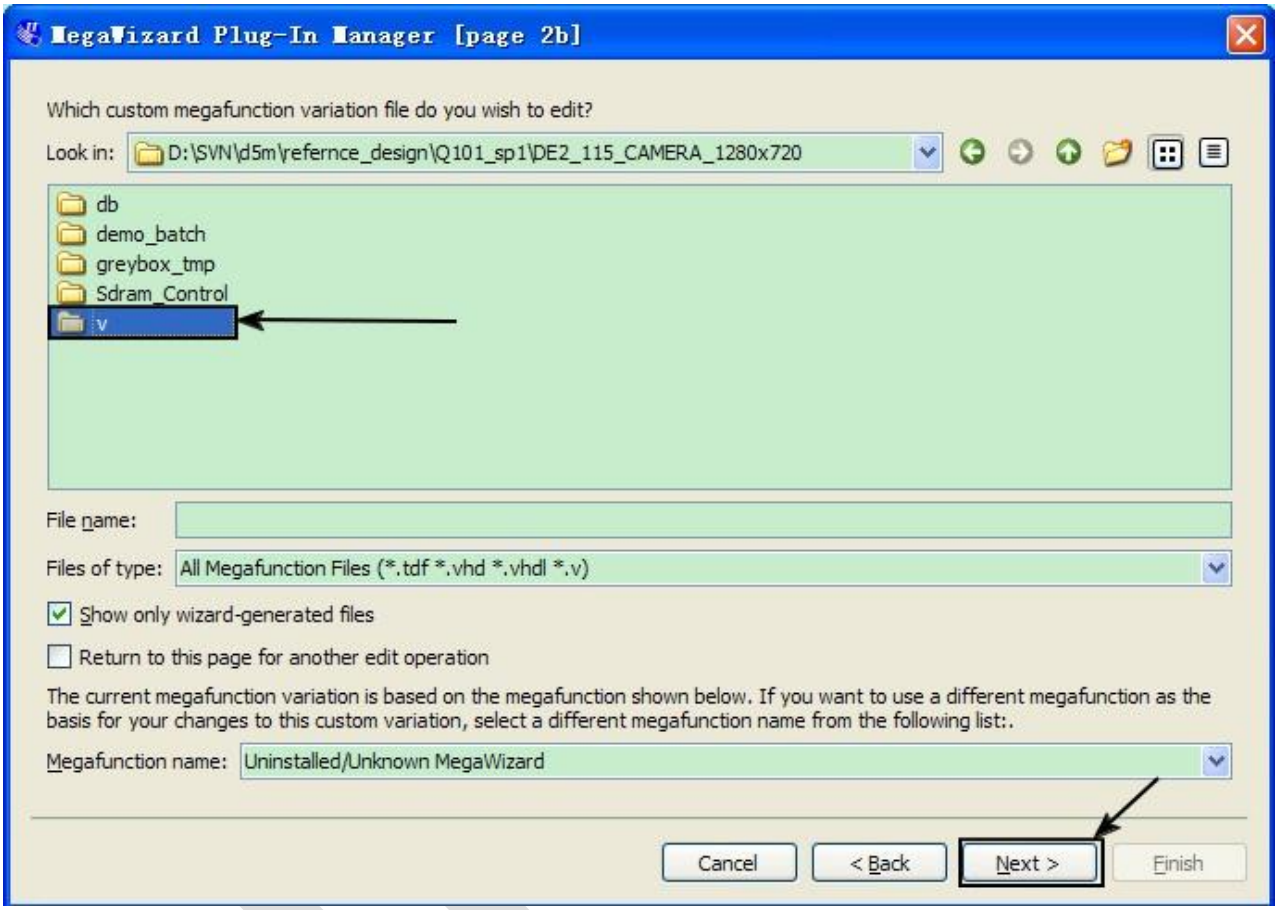
选择 Edit an existing custom megafunction variation 并点击 Next。

Choose Edit an existing custom megafunction variation, and then click Next.



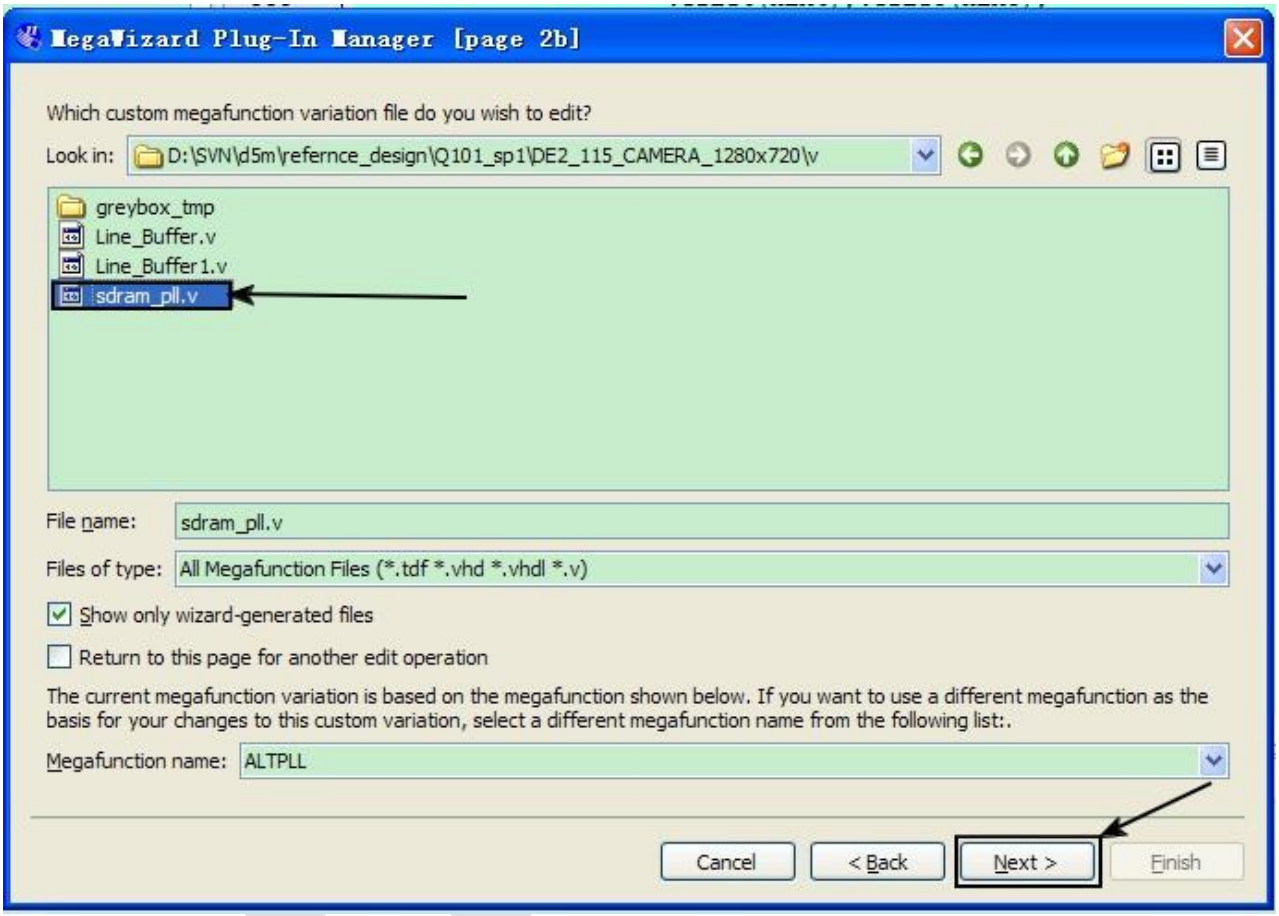
选择 v 文件夹，点击 Next。

Click the V folder, Next.



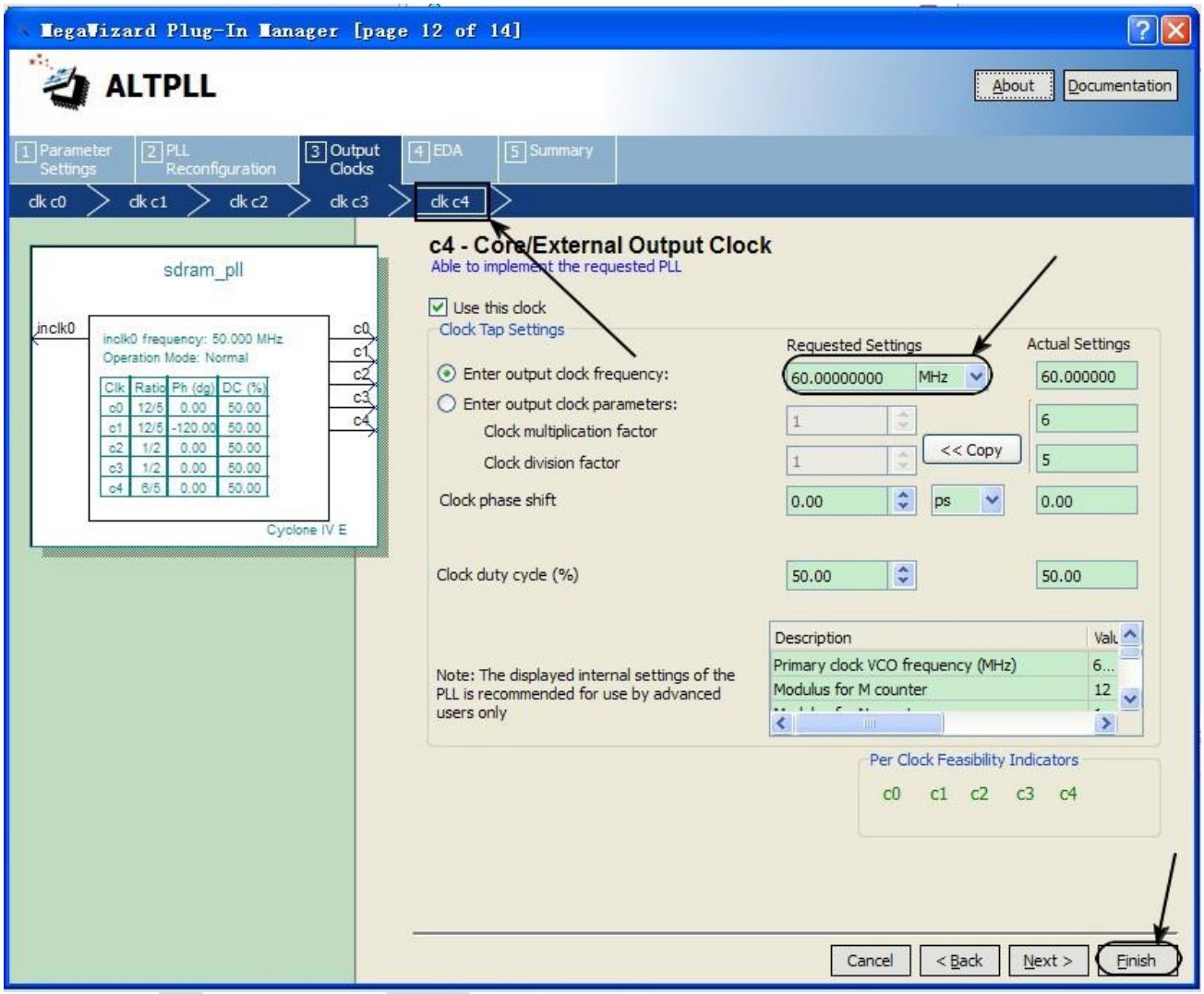
然后选择 sdram_pll.v 单击 Next。

Then choose sdram_pll.v, click Next.



把 clk c4 设置成 60M，点击 Finish。

Set clk c4 to 60M, click Finish.



2. SDRAM 的频率参数设置

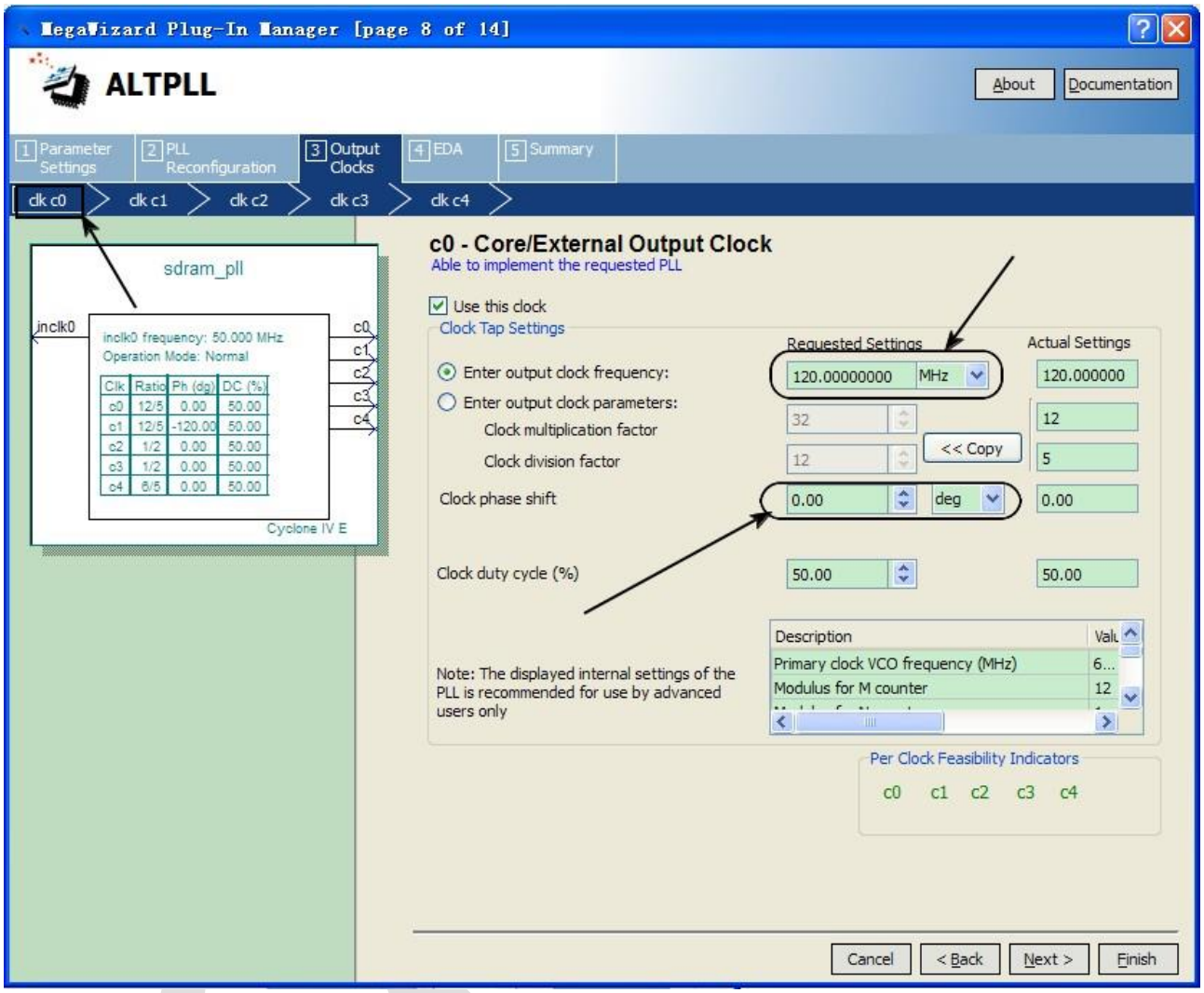
将原来的 100M 提升置 120M，可以再稍微调节一下相移设置成-125deg。

2 The parameters setting for the SDRAM frequency

Update the original 100MHz clk to 120MHz, set the clock phase shift to -125deg (it is optional)

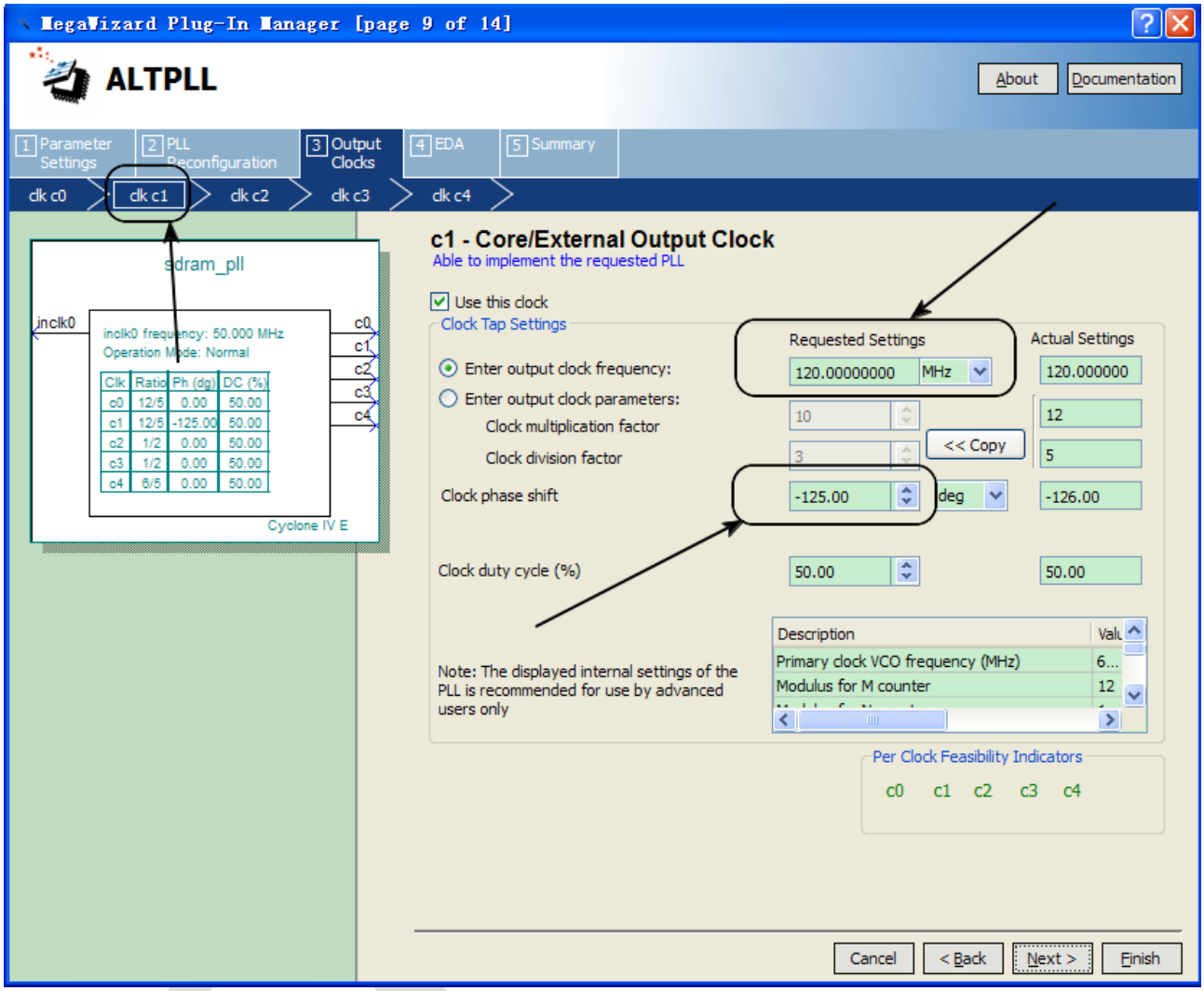
在 PLL 中将 clk c0 设置成 120M。

Set the clk c0 to 120MHz in PLL.



在 PLL 中将 c1 设置成 120M 并且设置 clock phase shift 位-125deg。

Set c1 to 120MHz and clock phase shift to -125deg.



1. Frame buffer 设置

1. Frame buffer setting

改分辨率以后需要重新修正 Fram buffer 宽度，打开 DE2_115_CAMERA.v 档，在 Sdram_Control u7（...）这里面修改如下：（

After updating the parameters for the resolution, the user needs to modify the width of the Frame Buffer. Open the DE2_115_CAMERA.v file, in the Sdram_Control u7 module, please make the modification: (

.WR1_MAX_ADDR(1280*720/2),

.WR2_MAX_ADDR(23'h100000+1280*720/2),

.RD1_MAX_ADDR(1280*720/2),

.RD2_MAX_ADDR(23'h100000+1280*720/2),

4.设置 ccd capture 的参数与 line buffer

4. Set the parameters of the CCD capture and the Line Buffer.
打开 V 文件夹里的 CCD_Capture.v 在里面设置：Parameter COLUMN_WIDTH = 1280;

再打开 v 文件夹中的 Line_Buffer.v 做如下修改：

Open the CCD_Capture.v file, and set Parameter COLUMN_WIDTH = 1280; then in the Line_Buffer.v file, make the modification as below:

defparam

altshift_taps_component.lpm_hint = "RAM_BLOCK_TYPE=M9K",

altshift_taps_component.lpm_type = "altshift_taps",

altshift_taps_component.number_of_taps = 3,

altshift_taps_component.tap_distance = 1280,

altshift_taps_component.width = 12;

5.相机设置

先设置好相机采集图像的行宽与列宽，然后去调节 piex 的频率，这时侯可以得到不稳定的图像（1.频率给太高只能踩到亮点。2.是由于 sdram 带宽有限会出现噪点）。

5. Camera Configuration

The user should default a proper width for the Row and Column, then to adjust the pixel frequency to get an unstable image. (1.If the frequency is too high, only high spot can be captured. 2. Should be note the limited of the sdram bandwidth to avoid noise appearance.)

打开 v 文件夹下的 I2C_CCD_Config.v 做如下修改：

Open I2C_CCD_Config.v file and update:

```
assign sensor_row_size=24'h03059F;

assign sensor_column_size=24'h0409FF;

assign sensor_row_mode = 24'h220011;

assign sensor_column_mode= 24'h230011;

assign sensor_start_row= 24'h010032;

assign sensor_start_column=24'h020000;
```

上述配置是将采集图像的规格设置成 1280X720.

From the parametes modification above, the captured image Specification has been set as 1280X720.

11 : LUT_DATA <= 24'h111A03; // PLL_m_Factor<<8+PLL_n_Divider

12 : LUT_DATA <= 24'h120003; // PLL_p1_Divider

以上参数是修改 D5M 的 PLL 值确定 piex 的频率，如上所述是在给定的频率是 25M 的情况下得到的 piex 频率为 40.625M。（建议在修改的时候建议先设置一个较低的频率看图像的稳定程度，再修改直到图像稳定。）

After the modification, the D5M has updated a PLL which can be used to generate the pixel clock internally. Take above parameters as an example, the pixel frequency will be 40.625MHz if the PLL frequency set as 25MHz. (Suggest the user to set a low frequency at the beginning then update the parameters until to get a stable image).

在图像稳定的基础上，由于 DE2_115SDRAM 带宽限制，会出现噪点的问题，需要设置一下 H_BALNKING 和 V_BLANKING 直到图像与拍摄的图像一致。

Due to the bandwidth limited of DE2_115SDRAM, there will be come out the niose after these modifications. In order to get the stable output on image, the user needs to reset the H_BALNKING & V_BLANKING values to get accordance of the image output to the image caputer.

3 : LUT_DATA <= 24'h050078; // H_Blanking Legal values: [0, 4095].

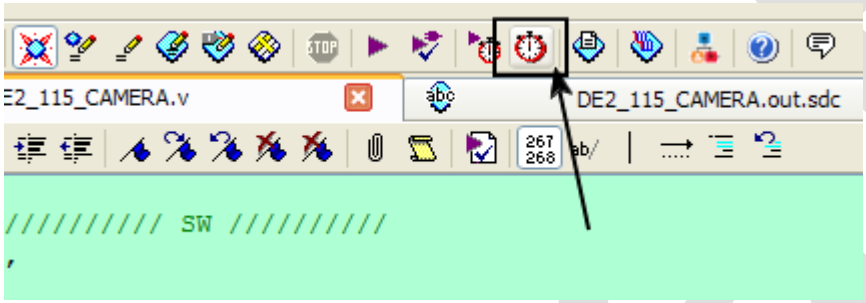
4 : LUT_DATA <= 24'h060008; // V_Blanking Legal values: [8, 2047].

6.创建和添加 SDC 文件

6. Create and add the SDC file.

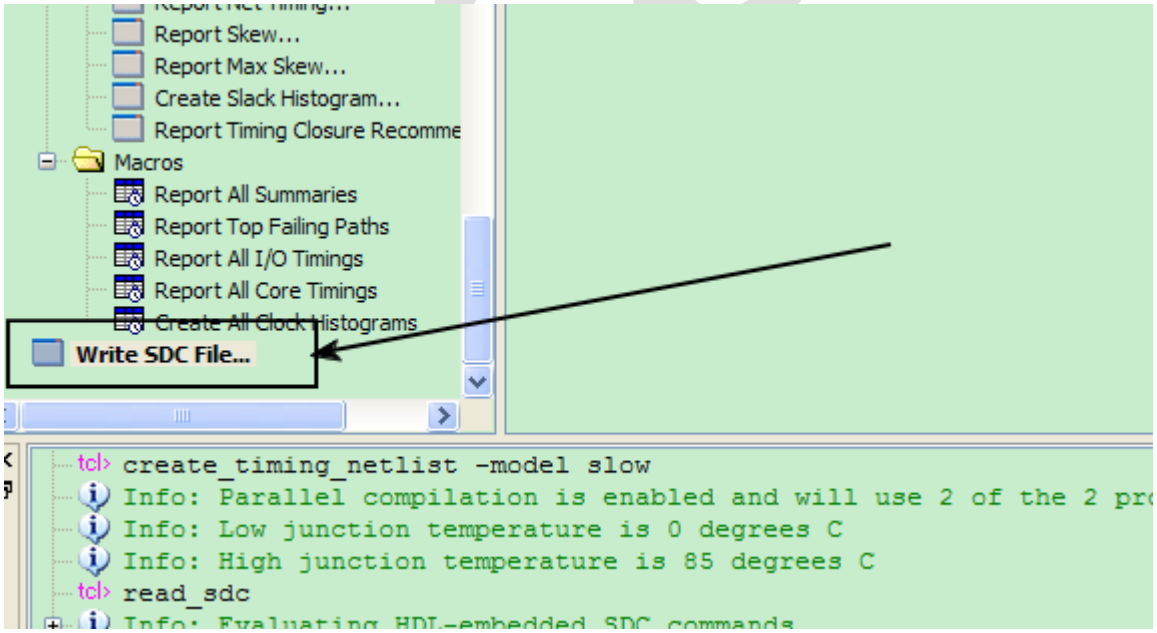
点击 timingquest timimg analyzer。

Click timingquest timimg analyzer

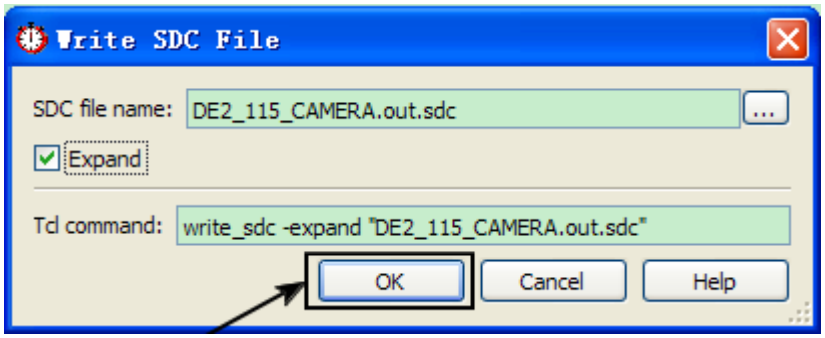


点击 WRITE sdc FILE…

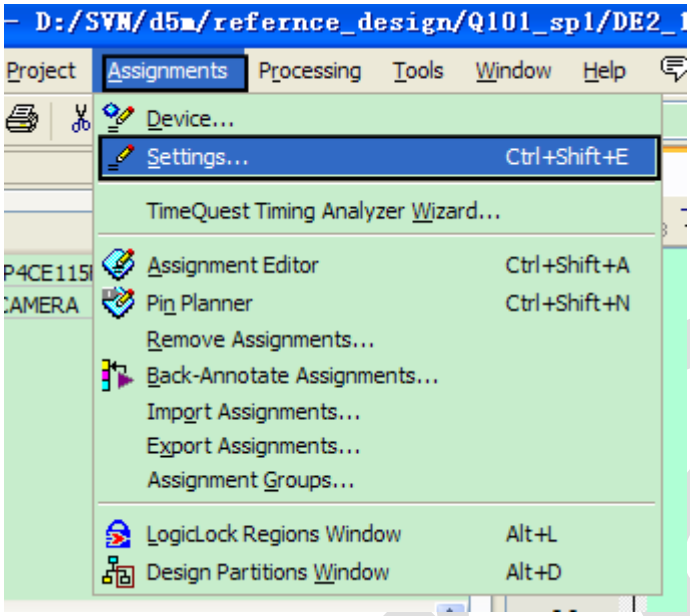
Click WRITE sdc FILE…



Click OK

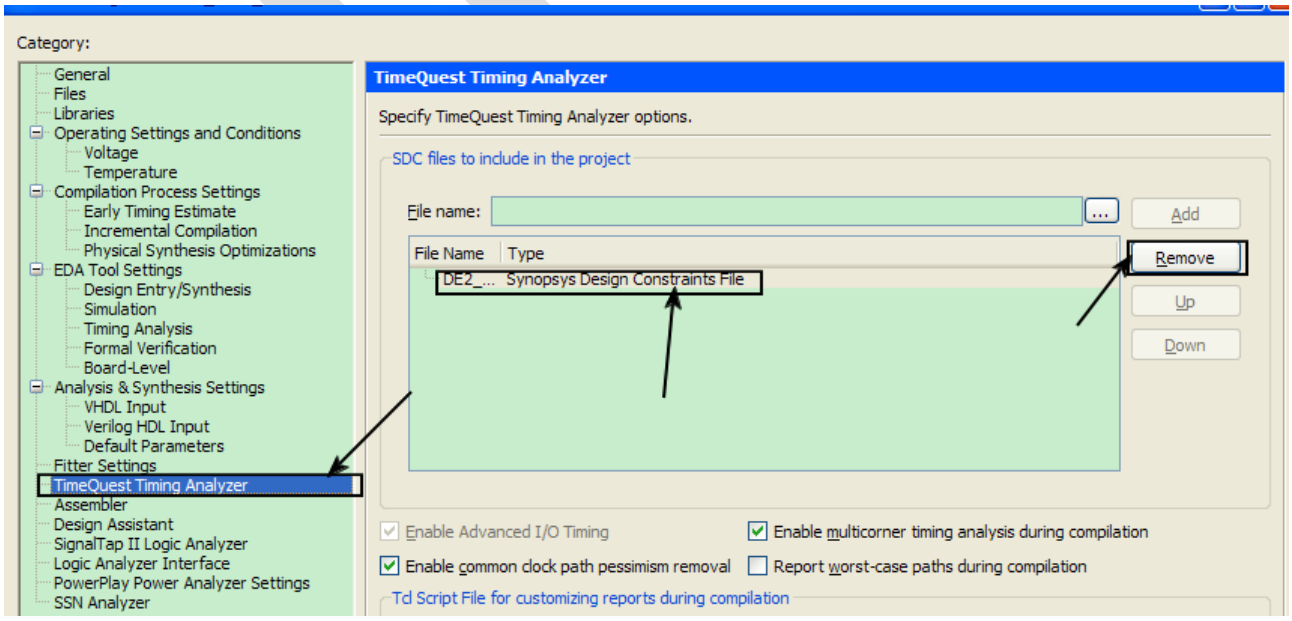


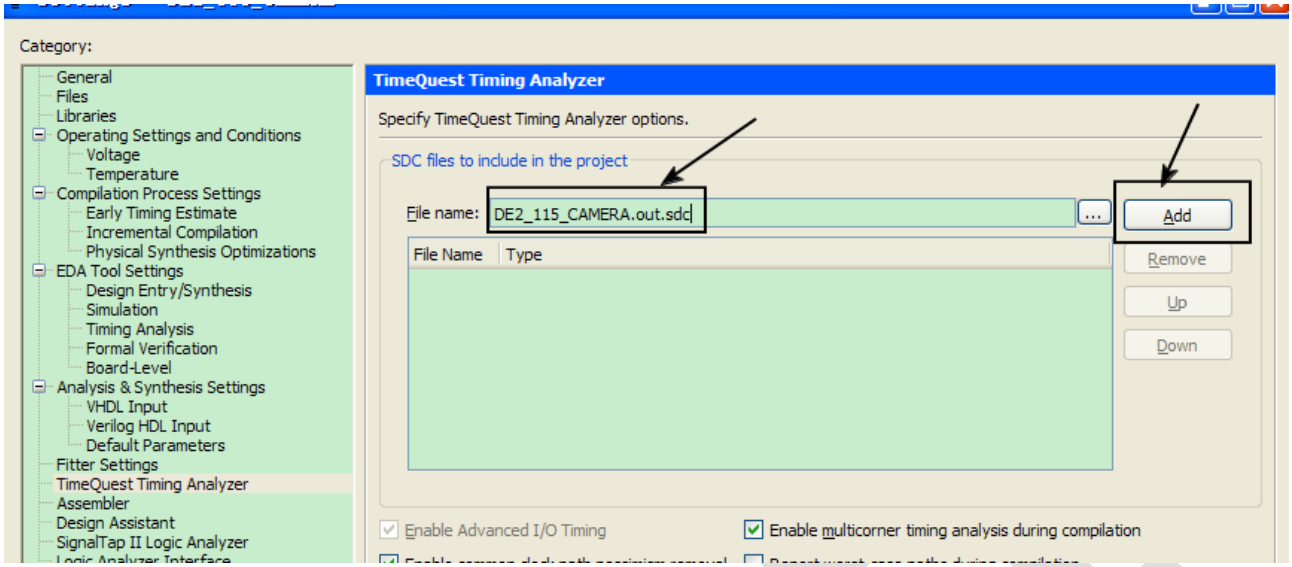
Then Click assignment > setting



点击到 timequest Timing analyzer 将原来的 SDC File remove 掉并添加刚才生成的 SDC 文件。

Click the timequest Timing analyzer button, remove the original SDC File and add the new one.





然后点击 aapply 点击 OK。

新编译并且下载。

Click apply, then OK

Compile the project once again then download.